In the Specification

Please substitute the following amended paragraph for the paragraph beginning on page 7, line 21:

FIGs. 4A to 4F are cross-sections of FIG. 3 along line 1-1, showing the fabrication process of the interconnect structure in the non-display area II of the TFT-array substrate 300. As shown in FIG. 4A, a metal line 310 is disposed in the non-display area II of TFT array substrate 300. The metal line 310 can be simultaneously formed with gate metal lines, e.g. a Ti-Al-Ti laminated layer of a thickness about 2500Å, of the TFT array on the display area of substrate ~~100~~ 300. An insulating layer 320, e.g. a SiNx layer of a thickness about 3000Å, is then formed, covering the metal line 310 and the exposed surface of the substrate 300. Another metal line 330 is then formed on the insulating layer 320. Preferably, one end (310a) of the metal line 310 overlaps with, crosses, or is close to one end (330a) of the metal line 330 for subsequent interconnection. The metal line 330 can be simultaneously formed with source/drain metal lines of the TFT array in the display area I of substrate 300, which can be a Ti-Al-Ti laminated layer of a thickness about 2500Å. Another insulating layer 340 is then formed, covering the metal line 330 and the insulating layer 320. The insulating layer 340 can also be a SiNx layer with thickness about 3000Å. After the metal lines 310 and 330 are formed, a passivation layer 350 is deposited on the insulating layer 340. A thick passivation layer 350 is formed to cover the surface of the insulating layer 340, preferably an organic layer with a thickness of 3-4μm.